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CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A method, comprising:

receiving a legacy type hardware interrupt request ("IRQ") by a processor during a native mode runtime of the processor;

invoking at least one legacy type interrupt service routine ("ISR") by a global interrupt handler to service the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ ~~received during the native mode runtime~~,

wherein invoking the at least one legacy type ISR includes transitioning from the native mode runtime to a legacy mode runtime in response to the legacy type hardware IRQ to service the legacy type hardware IRQ,

wherein the native mode runtime is a higher performance state of the processor than [[a]] the legacy mode runtime of the processor defined by a number of bits processed in parallel.

2. (Cancelled)

3. (Currently Amended) The method of claim [[2]] 1 wherein servicing the legacy type hardware IRQ includes:

executing the at least one legacy type ISR; and

returning to the native mode runtime prior to servicing another legacy type hardware IRQ.

4. (Previously Presented) The method of claim 3 wherein the global interrupt handler comprises a native type ISR.

5. (Original) The method of claim 3, further comprising:

copying the at least one legacy type ISR from a firmware unit to system memory; and

servicing the legacy type hardware IRQ with the copied at least one legacy type ISR executed from the system memory.

6. (Original) The method of claim 1, further comprising:

receiving a native type hardware IRQ by the processor during the legacy mode runtime of the processor;

transitioning from the legacy mode runtime to the native mode runtime in response to the native type hardware IRQ; and

servicing the native type hardware IRQ.

7. (Original) The method of claim 1 wherein the legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

8. (Previously Presented) The method of claim 1 wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code or 64-bit

code and wherein the native mode runtime of the processor includes executing one of 32-bit code or 64-bit code by the processor.

9. (Original) The method of claim 1, further comprising:

receiving a legacy type hardware IRQ by the processor during the legacy mode runtime;

transitioning to the native mode runtime in response to the legacy type hardware IRQ to determine a type of the legacy type hardware IRQ;

transitioning back to the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ during the legacy mode runtime of the processor.

10. (Currently Amended) A tangible machine-accessible medium that provides instructions that, if executed by a machine, will cause the machine to perform operations comprising:

receiving a legacy type hardware interrupt request ("IRQ") by a processor of the machine during a native mode runtime of the processor;

invoking at least one legacy type interrupt service routine ("ISR") by an interrupt handler to service the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ ~~received during the native mode runtime~~,

wherein invoking the at least one legacy type ISR includes transitioning from the native mode runtime to a legacy mode runtime in response to the legacy type hardware IRQ to service the legacy type hardware IRQ,

wherein the native mode runtime is a higher performance state of the processor than [[a]] the legacy mode runtime of the processor defined by a number of bits processed in parallel.

11. (Cancelled)

12. (Currently Amended) The machine-accessible medium of claim [[11]] 10, further embodying instructions that, if executed by the machine, will cause the machine to perform the operations wherein servicing the legacy type hardware IRQ includes:

executing the at least one legacy type ISR; and

returning to the native mode runtime prior to servicing another legacy type hardware IRQ.

13. (Previously Presented) The machine-accessible medium of claim 12, wherein the global interrupt handler comprises a native type ISR.

14. (Original) The machine-accessible medium of claim 12, further embodying instructions that, if executed by the machine, will cause the machine to perform operations, further comprising:

copying the at least one legacy type ISR from a firmware unit to system memory; and

servicing the legacy type hardware IRQ with the copied at least one legacy type ISR executed from the system memory.

15. (Original) The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform operations, further comprising:

receiving a native type hardware IRQ by the processor during the legacy mode runtime of the processor;

transitioning from the legacy mode runtime to the native mode runtime in response to the native type hardware IRQ; and

servicing the native type hardware IRQ.

16. (Original) The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform the operations wherein the legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

17. (Previously Presented) The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform the operations wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code or 64-bit code and wherein the native mode runtime of the processor includes executing one of 32-bit code or 64-bit code by the processor.

18. (Original) The machine-accessible medium of claim 10, further embodying instructions that, if executed by the machine, cause the machine to perform operations, further comprising:

receiving a legacy type hardware IRQ by the processor during the legacy mode runtime;

transitioning to the native mode runtime in response to the legacy type hardware IRQ to determine a type of the legacy type hardware IRQ;

transitioning back to the legacy type hardware IRQ; and

servicing the legacy type hardware IRQ during the legacy mode runtime of the processor.

19. – 28. (Cancelled)

29. (Currently Amended) A processing system, comprising

a processor coupled to receive a hardware interrupt request ("IRQ"); and

at least one machine-accessible medium that provides instructions that, if executed by the processor, will cause the processor to perform operations comprising:

receiving the hardware IRQ;

determining whether the hardware IRQ is a native type hardware IRQ or a legacy type hardware IRQ with an interrupt handler;

invoking at least one legacy type interrupt service routine ("ISR") to service the hardware IRQ, if the hardware IRQ is determine to be a legacy type hardware IRQ received during a native mode runtime of the processor,

wherein invoking the at least one legacy type ISR to service the hardware IRQ, includes transitioning from the native mode runtime to a legacy mode runtime in response to the legacy type hardware IRQ to service the legacy type hardware IRQ,

wherein the native mode runtime is a higher performance state of the processor than [[a]] the legacy mode runtime of the processor defined by a number of bits processed in parallel; and

invoking at least one native type ISR to service the hardware IRQ, if the hardware IRQ is determine to be a native type hardware IRQ received during the native mode runtime.

30. (Previously Presented) The processing system of claim 29, wherein the interrupt handler comprises a native type ISR.

31. (Cancelled)

32. (Currently Amended) The processing system of claim [[31]] 29 wherein the at least one machine-accessible medium provides further instructions that, if executed by the processor, will cause the processor to perform further operations comprising:

returning the processor to the native mode runtime after executing the at least one legacy type ISR and prior to executing another legacy type ISR in response to another legacy type hardware IRQ.

33. (Currently Amended) The processing system of claim 29 wherein the at least one machine-accessible medium provides further instructions that, if executed by the processor, will cause the processor to perform further operations comprising:

~~transition~~ transitioning from the legacy mode runtime to the native mode runtime in response to receiving the hardware IRQ, if the hardware IRQ is received by the processor during the legacy mode runtime.

34. (Previously Presented) The processing system of claim 33, further comprising:

system memory communicatively coupled to the processor and coupled to receive a copy of the at least one native type ISR and a copy of the at least one legacy type ISR from the at least one non-volatile memory unit, the processor to execute the copy of the at least one native type ISR and the copy of the at least one legacy type ISR from the system memory.

35. (Currently Amended) The processing system of claim 34 wherein the interrupt handler comprises a global interrupt handler, the global interrupt handler to be transferred into the system memory and executed therefrom. [[,]]

36. (Previously Presented) The processing system of claim 29 wherein the legacy type hardware IRQ includes an IRQ from a hardware entity that executes 16-bit code and wherein the legacy mode runtime of the processor includes executing 16-bit code by the processor.

37. (Previously Presented) The processing system of claim 29 wherein the native type hardware IRQ includes an IRQ from an entity that executes one of 32-bit code or 64-bit code and wherein the native mode runtime of the processor includes executing one of 32-bit code or 64-bit code by the processor.